AMENDMENTS TO THE CLAIMS

Claims 1-45. (Canceled)

46. (Currently amended) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate such that ~~at least a portion of a top surface of~~ said buried conductor pattern is below a top surface of said substrate and said buried conductor pattern is completely surrounded by the same monocrystalline substrate material of said monocrystalline substrate ~~at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate~~, said at least one buried conductor pattern ~~having a spherical pattern and~~ forming at least a part of an interconnect between devices, and a conductive path extending from said buried conductor pattern to said devices, wherein at least a portion of said conductive path extends below said top surface of said substrate.

47. (Previously presented) The integrated circuit of claim 46, further comprising a second buried conductor pattern having a pipe-shaped pattern.

48. (Previously presented) The integrated circuit of claim 46, further comprising a second buried conductor pattern having a plate-shaped pattern.

Claims 49-50 (Canceled).

51. (Previously presented) The integrated circuit of claim 46, wherein said at least one buried conductor pattern is formed of a material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum and aluminum alloy.

52. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon substrate.

53. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a germanium substrate.

54. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon-on-insulator substrate.

55. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon-on-nothing substrate.

56. (Currently amended) A buried conductor pattern within a monocrystalline substrate, comprising:

at least one empty-spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein~~, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration~~;

a conductive material filling said empty space pattern such that ~~at least a portion of a top surface of~~ said conductive material is below a top surface of said monocrystalline substrate and said at least one empty-spaced pattern is completely surrounded by the same monocrystalline substrate material of said monocrystalline substrate ~~at least a portion of a bottom surface of said conductive material is above a bottom surface of said monocrystalline substrate~~, said buried conductor pattern forming at least a part of an interconnect between devices ~~and being completely surrounded by monocrystalline material~~; and

a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate, wherein at least a portion of said conductive path extends below said top surface of said substrate.

Claim 57. (Canceled)

58. (Original) The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a pipe-shaped configuration.

59. (Original) The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a plate-shaped configuration.

60. (Original) The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a sphere-shaped configuration.

61. (Canceled)

62. (Currently amended) A processor system comprising:

a processor; and

a circuit coupled to said processor, at least one of said circuit and processor comprising:

a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said monocrystalline substrate having at least one hole drilled therein~~, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration~~;

a conductive material filling said empty space pattern such that ~~at least a portion of a top surface of~~ said conductive material is below a top surface of said

monocrystalline substrate and said conductive structure is completely surrounded by the same monocrystalline substrate material of said monocrystalline substrate ~~at least a portion of a bottom surface of said conductive material is above a bottom surface of said monocrystalline substrate~~, said conductive structure forming at least a part of an interconnect between devices ~~and being completely surrounded by monocrystalline material~~; and

a conductive path extending from said conductive structure to said top surface of said monocrystalline substrate, wherein at least a portion of said conductive path extends below said top surface of said substrate.

63. (Previously presented) The processor based system of claim 62, wherein said empty-spaced pattern has a pipe-shaped configuration.

64. (Original) The processor system of claim 62, wherein said empty-spaced pattern has a plate-shaped configuration.

65. (Original) The processor system of claim 62, wherein said empty-spaced pattern has a sphere-shaped configuration.

66. (Canceled)

67. (Original) The processor system of claim 62, wherein said circuit is a memory circuit.

68. (Original) The processor system of claim 62, wherein said circuit is a DRAM memory circuit.

69. (Original) The processor system of claim 62, wherein said circuit and said processor are integrated on same circuit.

70. (Original) The processor system of claim 62, wherein said processor comprises said conductive structure.

71. (Original) The processor system of claim 62, wherein said circuit comprises said conductive structure.

72. (Currently amended) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate such that ~~at least a portion of a top surface of~~ said buried conductor pattern is below a top surface of said substrate and said buried conductor pattern is completely surrounded by the same monocrystalline substrate material of said monocrystalline substrate ~~at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate~~, said at least one buried conductor pattern ~~having a plate-shaped pattern and~~ forming at least a part of an interconnect between devices, and a conductive path extending from said buried conductor pattern, wherein at least a portion of said conductive path extends below said top surface of said substrate.

73. (Previously presented) The integrated circuit of claim 72, further comprising a second buried conductor pattern having a pipe-shaped pattern.

74. (Previously presented) The integrated circuit of claim 73, further comprising a third buried conductor pattern having a spherical pattern.

75. (Currently amended) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate such that ~~at least a portion of a top surface of~~ said buried conductor pattern is below a top surface of said substrate and said buried conductor pattern is completely surrounded by the same monocrystalline material of said monocrystalline substrate ~~at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate~~,

said at least one buried conductor pattern ~~having a pipe-shaped pattern and~~ forming at least a part of an interconnect between devices, and a conductive path extending from said buried conductor pattern, wherein at least a portion of said conductive path extends below said top surface of said substrate.

76. (Currently amended) An integrated circuit substrate comprising first and second buried conductor patterns provided within a monocrystalline substrate such that ~~at least a portion of a top surface of each of~~ said buried conductor patterns [[is]] are below a top surface of said substrate and said buried conductor patterns are completely surrounded by the same monocrystalline material of said monocystalline substrate ~~at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate~~, said first and second buried conductive patterns forming at least a part of first and second interconnects between devices, respectively, wherein said first buried conductor pattern is located below said second buried conductor pattern and relative to said surface of said monocrystalline substrate, and a first conductive path extending from said first buried conductor pattern and a second conductive path extending from said second buried conductor pattern, wherein at least a portion of said conductive paths extend below said top surface of said substrate.

77. (Previously presented) The integrated circuit of claim 76, further comprising a third buried conductor pattern located below said first and second buried conductor patterns and relative to a surface of said monocrystalline substrate and a third conductive path extending from said third buried conductor pattern.

78. (Previously presented) The integrated circuit of claim 77, wherein one of said buried conductor patterns has a pipe-shaped pattern.

79. (Previously presented) The integrated circuit of claim 77, wherein one of said buried conductor patterns has a plate-shaped pattern.

80. (Previously presented) The integrated circuit of claim 77, wherein one of said buried conductor patterns has a spherical pattern.

81. (Previously presented) The integrated circuit of claim 77, wherein said buried conductor patterns are formed of a conductive material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum and aluminum alloy.

82. (Withdrawn) A buried conductive structure provided within a semiconductor substrate, said buried conductive structure being formed by a method comprising the steps of:

forming at least one empty-spaced pattern beneath a surface of, and within a, semiconductor substrate, said empty-spaced pattern being surrounded by semiconductor material;

forming at least one opening within said semiconductor substrate, said opening connecting a respective empty-spaced pattern with the exterior of said semiconductor substrate; and

forming a conductive material in said empty-spaced pattern and said opening.

83. (Withdrawn) The buried conductive structure of claim 82, wherein the act of forming said empty-spaced pattern further comprises the act of forming at least one hole within said semiconductor substrate and heat treating said substrate to form said empty-spaced pattern beneath said surface of said semiconductor material.

84. (Withdrawn) The buried conductive structure of claim 83, wherein said hole is a cylindrical hole.

85. (Withdrawn) The buried conductive structure of claim 82, wherein said empty-spaced pattern has a pipe-shaped configuration.

86. (Withdrawn) The buried conductive structure of claim 82, wherein said empty-spaced pattern has a spherical configuration.

87. (Withdrawn) The buried conductive structure of claim 82, wherein said empty-spaced pattern has a plate-shaped configuration.

88. (Withdrawn) The buried conductive structure of claim 82, wherein said at least one empty-spaced pattern comprises at least one pipe-shaped pattern and at least one plate-shape pattern.

89. (Withdrawn) The buried conductive structure of claim 88, wherein said at least one pipe-shaped pattern and said at least one plate-shape pattern are formed simultaneously.

90. (Withdrawn) The buried conductive structure of claim 89, wherein said at least one pipe-shaped pattern and said at least one plate-shape pattern are formed sequentially and before said act of forming said conductive material.

91. (Withdrawn) The buried conductive structure of claim 82, wherein said conductive material is formed of a material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum, and aluminum alloy.